```
     (FILE 'USPAT' ENTERED AT 14:48:48 ON 21 APR 1999)
L1         53202 S (DATA OR DMA) (2A) TRANSFER###
L2        389269 S BURST# OR WORD# OR PACKET# OR (PREDETERMIN#### (2A) NUMB
ER
L3        216931 S INTERRUPT###
L4                QUE CONTINUOUS##
L5           73 S L4 (P) L1 (P) L2 (P) L3
L6         5202 S (CHECK? OR DETERMIN###) (3A) (L3)
L7         7427 S 'AFTER' (3W) L2
L8            1 S L6 (10A) L7
L9         7704 S ACCESS (4A) REQUEST#
L10           4 S L7 (10A) L9
L11               QUE TIMER OR TIME
L12               QUE WITHOUT
L13       25630 S L12 (5W) L11
L14         464 S L13 (10A) L3
L15           1 S L13 (P) L1 (P) L9 (P) L2
```

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L11               QUE TIMER OR TIME
L12               QUE WITHOUT
L13       25630 S L12 (5W) L11
L14         464 S L13 (10A) L3
L15           1 S L13 (P) L1 (P) L9 (P) L2
L16        1492 S RELEAS? (4A) BUS
L17           5 S L16 (P) L7
L18               QUE (RELINQU? OR FREE####) (4A) BUS
L19          23 S L18 (P) L7

     FILE 'EPO' ENTERED AT 16:56:55 ON 21 APR 1999
L20           2 S L19
L21           0 S L17

     FILE 'JPO' ENTERED AT 16:58:48 ON 21 APR 1999
L22           0 S L17
L23           0 S L19
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6. 5,729,681, Mar. 17, 1998, Method of communicating data from a host to a network controller; Vikas Aditya, et al., 395/200.6; 709/213, 220, 236, 245, 250 [IMAGE AVAILABLE]

US PAT NO: 5,729,681 [IMAGE AVAILABLE] L5: 6 of 73

SUMMARY:

BSUM(28)

The . . . must be initiated to access each separate TBD. And the initiation of a new memory cycle is a limit on **burst** mode **transfer** of **data** from main memory. A **burst** is a **continuous transfer** of **data** without **interruption** from main memory to a controller. In a multiplexing bus, **burst** mode provides an efficient way to dedicate the bus for the transmission of data from one source. Also, a move. . . contention for the bus, a bus master device must give up the bus which is also a reduction of the

5. 4,490,788, Dec. 25, 1984, Well-logging data processing system having segmented serial processor-to-peripheral data links; Marvin W. Rasmussen, 710/21; 364/222.2, 223.8, 228.3, 232.8, 238.3, 239.51, 242.3, 242.31, 242.4, 242.5, 263, 284, DIG.1; 710/129 [IMAGE AVAILABLE]

US PAT NO: 4,490,788 [IMAGE AVAILABLE] L17: 5 of 5

DETDESC:

DETD(68)

If . . . and the processor interface unit 26 becomes bus master. The NPR/DMA cycle control logic 66 transfers one word of data. **After** the data **word** has been transferred, the NPR/DMA cycle control logic 66 drops BBSY to **release** the processor **bus** 12. This process is repeated until the entire message has been transferred.

1. 5,862,338, Jan. 19, 1999, Polling system that determines the status of network ports and that stores values indicative thereof; William J. Walker, et al., 395/200.54 [IMAGE AVAILABLE]

US PAT NO: 5,862,338 [IMAGE AVAILABLE] L17: 1 of 5

DETDESC:

DETD(168)

At . . . 226 provides the transmit control list to its transmit control list buffer 827b. At next step 870c, the TLAN 226 **releases** the PCI **bus** 222, but immediately re-requests the PCI bus 222 as indicated at step 870d. Once the TLAN 226 again receives control. . . and enabling the corresponding TPI TX FIFO and provides the data to the TLAN 226 across the PCI bus 222. **After** each data **burst**, the TLAN 226 releases control the of the PCI bus 222 as indicated at next step 871c. If transfer of. . .

2. 5,603,007, Feb. 11, 1997, Methods and apparatus for controlling back-to-back burst reads in a cache system; Farid A. Yazdy, et al., 711/140; 710/35; 711/3, 167 [IMAGE AVAILABLE]

US PAT NO: 5,603,007 [IMAGE AVAILABLE] L17: 2 of 5

CLAIMS:

CLMS(1)

We . . .
cache, for receiving a current cache address signal corresponding to a first burst read operation and maintaining said current signal **after** a second **burst** read operation is initiated and until the first burst read operation is completed; and
a bus translator unit coupled to the. . .
said address latch to maintain the current cache address signal, and then generates an address acknowledge signal which causes said **bus** master to **release** the current cache address signal and issue a subsequent cache address signal before the first burst read operation is completed.

3. 5,517,196, May 14, 1996, Smart blind spot sensor with object ranging; Allan G. Pakett, et al., 342/70, 71 [IMAGE AVAILABLE]

US PAT NO: 5,517,196 [IMAGE AVAILABLE] L17: 3 of 5

DETDESC:

DETD(45)

The . . . access) requests to the DSP 508 whenever it has a complete data word to be written to the RAM 506. **After** writing a data **word** to the RAM 506, the FPGA 504 **releases** the **bus** 509 and allows the DSP 508 to regain control of the bus 509.

4. 4,862,451, Aug. 29, 1989, Method and apparatus for switching information between channels for synchronous information traffic and asynchronous data packets; Felix H. Closs, et al., 370/353, 364, 413, 423

[IMAGE AVAILABLE]

US PAT NO: 4,862,451 [IMAGE AVAILABLE] L1 4 of 5

DETDESC:

DETD(30)

A . . . bus controller 25. This ends the CS slot portion of the frame. The PS window is then started by the **bus** controller 25, by **releasing** a token which is a particular bit sequence on the token loop line and by changing the CS/PS window indicator. . . unit which has a data packet ready for transmission. The token is released by the respective PS input port unit **after** the **packet** transmission, for further propagation on the token loop line 65, and may finally return to the bus controller 25 in. . .

5. 4,490,788, Dec. 25, 1984, Well-logging data processing system having segmented serial processor-to-peripheral data links; Marvin W. Rasmussen, 710/21; 364/222.2, 223.8, 228.3, 232.8, 238.3, 239.51, 242.3, 242.31, 242.4, 242.5, 263, 284, DIG.1; 710/129 [IMAGE AVAILABLE]

US PAT NO: 4,490,788 [IMAGE AVAILABLE] L17: 5 of 5

DETDESC:

DETD(68)

If . . . and the processor interface unit 26 becomes bus master. The NPR/DMA cycle control logic 66 transfers one word of data. **After** the data **word** has been transferred, the NPR/DMA cycle control logic 66 drops BBSY to **release** the processor **bus** 12. This process is repeated until the entire message has been transferred.

US PAT NO: 5,862,387 [IMAGE AVAILABLE] L19: 1 of 23

DETDESC:

DETD(51)

According to the single transfer mode, DMA controller 135 **relinquishes** control of primary **bus** 15 **after** each byte, **word**, or double word is transferred so that the processor 50 may have access to primary bus 15 on a regular basis. The single transfer mode is implicitly supported when a DMA agent immediately deasserts its REQ# signal after every transfer, or when DMA controller 135 deasserts the appropriate DACK# signal after every transfer such that primary bus 130 deasserts the GNT# signal of the DMA agent. A DMA agent may deassert its REQ# signal in response to the requesting secondary bus agent deasserting its DREQ# signal or in response to detecting deassertion of the GNT# s

1. US005584033A , Dec. 10, 1996, Apparatus and method for burst data transfer employing a pause at fixed data intervals; BARRETT, WAYNE M (US) , et al.,
INT-CL: [6] G06F13/28
EUR-CL: G06F13/28; G06F13/42

US005584033A L20: 1 of 2

ABSTRACT: . . .

ready to proceed. This cycle is repeated until the data transmission is complete. The sending and receiving devices do not **relinquish** control of the **bus** during a pause, and therefore are not required to re-initialize communications. In the preferred embodiment, **after** n data **words** have been transmitted, the sender and receiver toggle interlocking signals that accomplish a handshaking between the two devices. The sender. . .

2. EP000534529A1, Mar. 31, 1993, Apparatus and method for burst data transfer.employing a pause at fixed data intervals.; BARRETT, WAYNE MELVIN (US), et al.,
INT-CL: G06F13/28
EUR-CL: G06F13/28; G06F13/42

EP000534529A1 L20: 2 of 2

ABSTRACT: . . .

ready to proceed. This cycle is repeated until the data transmission is complete. The sending and receiving devices do not **relinquish** control of the **bus** during a pause, and therefore are not required to re-initialize communications. In the preferred embodiment, **after** n data **words** have been transmitted, the sender and receiver toggle interlocking signals that accomplish a handshaking between the two devices. The sender. . .